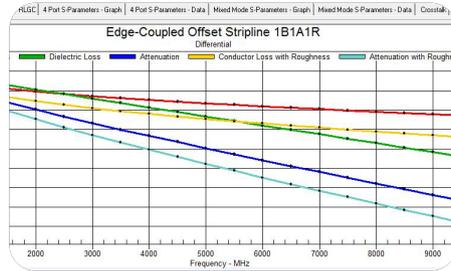
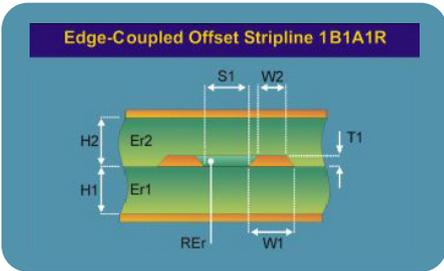
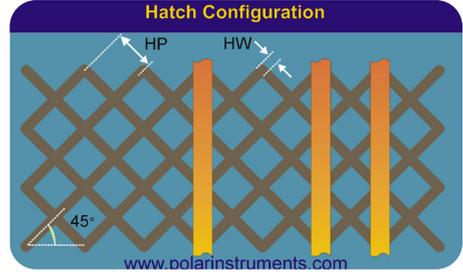
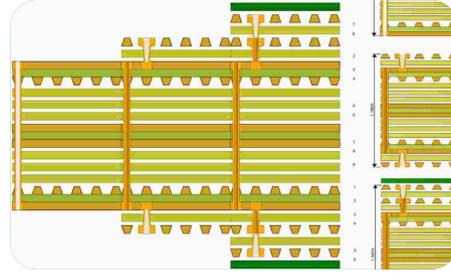
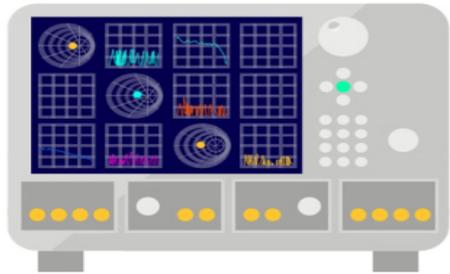
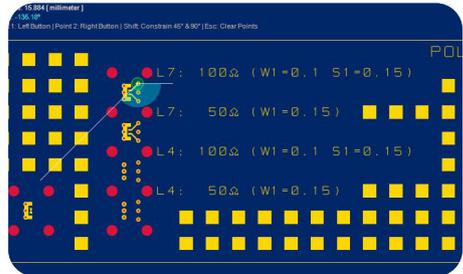




# Interconnected tools for PCB insertion loss



Speedstack Si - Stackup design  
Si9000e - Field solver  
CGen Si - Coupon generation  
Atlas Si for Touchstone



Improve communication efficiency

Resolve problems quickly

Predict manufacturing yield

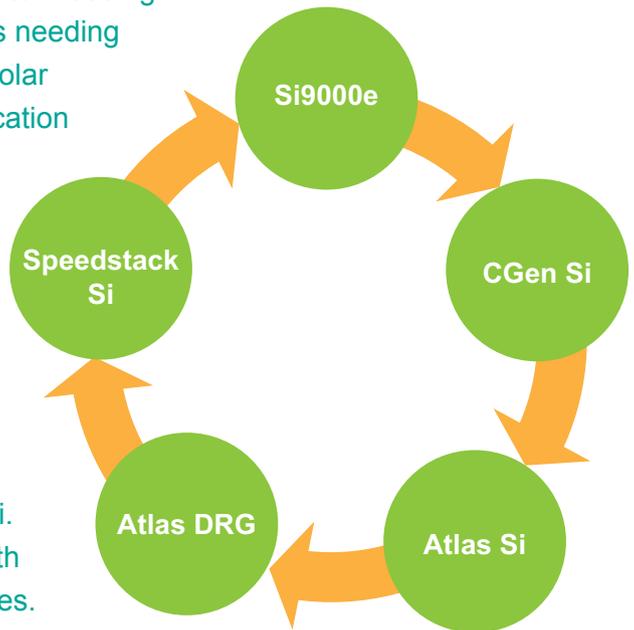
polarinstruments.com



## Design, specification and control of PCB insertion loss

As a PCB technologist, procurement engineer or fabricator needing to specify and design PCBs with ultra high speed traces needing control of insertion loss, you can benefit by deploying Polar interconnected tools for design, documentation, specification and test of insertion loss controlled PCBs. This Polar toolset is a popular solution for this task throughout the electronics supply chain – from prelayout stackup design, through to final insertion loss test.

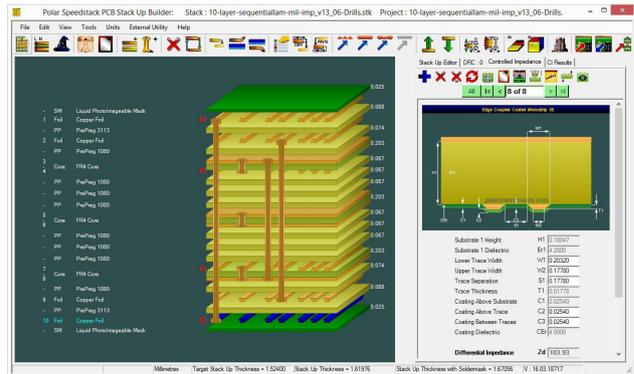
Starting with the Si9000e insertion loss field solver to explore your design space, you can specify and document using Speedstack Si. In addition, artwork for test coupons is then accurately generated with CGen Si. Speedstack Si also directly outputs stackups for use with CGen so it helps you generate insertion loss test vehicles. By selecting this suite of products throughout the supply chain you ease the communication from design through to fabrication – vitally important now that supply chains are now so extended.



## Speedstack Si

### Design and professionally document your PCB layer stackup

Speedstack Si gives the PCB technologist and fabricator a comprehensive suite of design and documentation tools to accurately realise even the most complex PCB layer stackups, including those that require specification of insertion loss. Speedstack Si also interfaces with high end CAD systems and allows you to share net classes. Speedstack Si links seamlessly with Si9000e, Atlas and CGen Si insertion loss coupon generator.

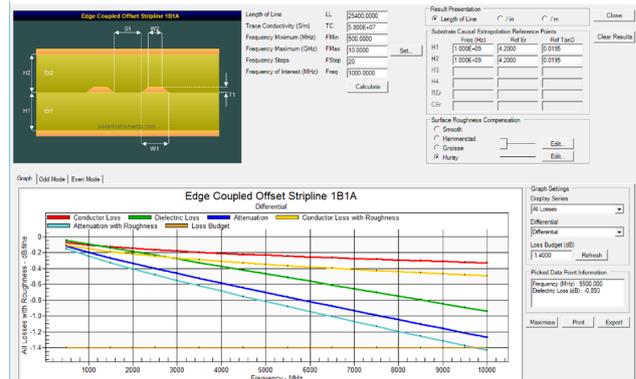


Layer	Stack-up	Material	Description	Layer	Predefined Thickness (mm)	±	Real Thickness (mm)	Trace Thickness (mm)	Predefined Thickness (mm)	±	Real Thickness (mm)	Trace Thickness (mm)	Predefined Thickness (mm)	±	Real Thickness (mm)	Trace Thickness (mm)
1	10	2000	Liquid Photoimageable Resin	10	0.050		0.050	0.050	0.050		0.050	0.050	0.050		0.050	0.050
2	9	PP	PrePreg 1500	9	0.076		0.076	0.076	0.076		0.076	0.076	0.076		0.076	0.076
3	8	PP	PrePreg 1500	8	0.076		0.076	0.076	0.076		0.076	0.076	0.076		0.076	0.076
4	7	PP	PrePreg 1500	7	0.076		0.076	0.076	0.076		0.076	0.076	0.076		0.076	0.076
5	6	PP	PrePreg 1500	6	0.076		0.076	0.076	0.076		0.076	0.076	0.076		0.076	0.076
6	5	PP	PrePreg 1500	5	0.076		0.076	0.076	0.076		0.076	0.076	0.076		0.076	0.076
7	4	PP	PrePreg 1500	4	0.076		0.076	0.076	0.076		0.076	0.076	0.076		0.076	0.076
8	3	PP	PrePreg 1500	3	0.076		0.076	0.076	0.076		0.076	0.076	0.076		0.076	0.076
9	2	PP	PrePreg 1500	2	0.076		0.076	0.076	0.076		0.076	0.076	0.076		0.076	0.076
10	1	2000	Liquid Photoimageable Resin	1	0.050		0.050	0.050	0.050		0.050	0.050	0.050		0.050	0.050

# Speedstack Si

## Model insertion loss within Speedstack

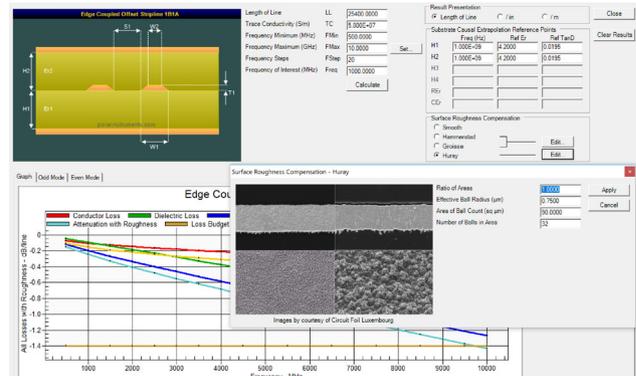
The new GHz capability in Speedstack Si allows you to fully model insertion loss – dielectric and copper losses and total attenuation. All the additional parameters for loss may be saved in the stackup files, and shared at any time with Si9000e for further analysis.



# Speedstack Si

## Account for copper roughness

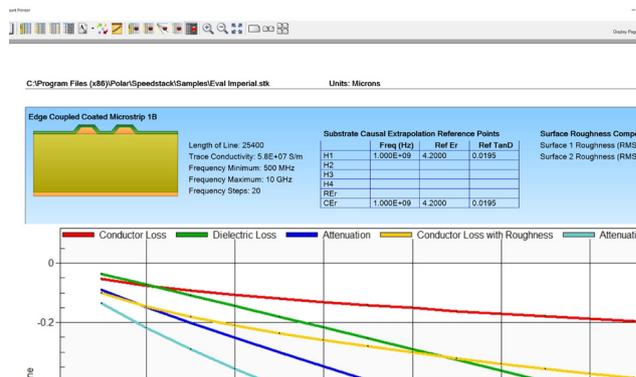
Copper roughness modeling is included in Speedstack Si, you can choose from industry standard models for copper loss calculation, Hammerstad, Gradient and Huray along with baseline calculations for smooth copper. The Huray method supports a Cannonball – Simonovich input processor for easy input of Huray parameters where access to SEM images is unavailable. All parameters can be pasted to and from Si9000e for further analysis.



# Speedstack Si

## Insertion loss documentation in reports

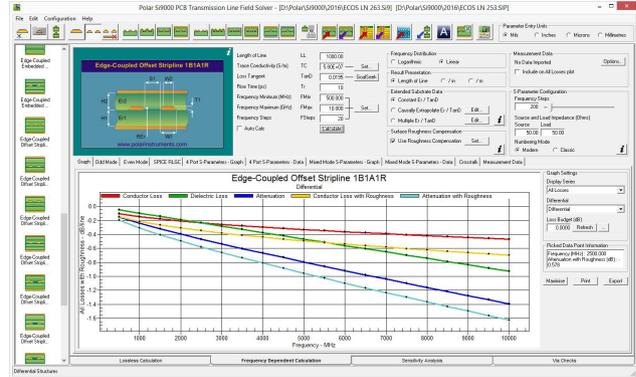
The Speedstack report can be configured to provide the appropriate level of information for fabricators, designers and technologists. It allows you to specify not only material types and stackup construction but also both characteristic impedance and insertion loss plots accounting for dielectric, copper and copper roughness. All the insertion loss information contained in the Speedstack file is easily shared with the Si9000e insertion loss field solver for easy analysis.



# Si9000e

## Field solving PCB transmission line design system

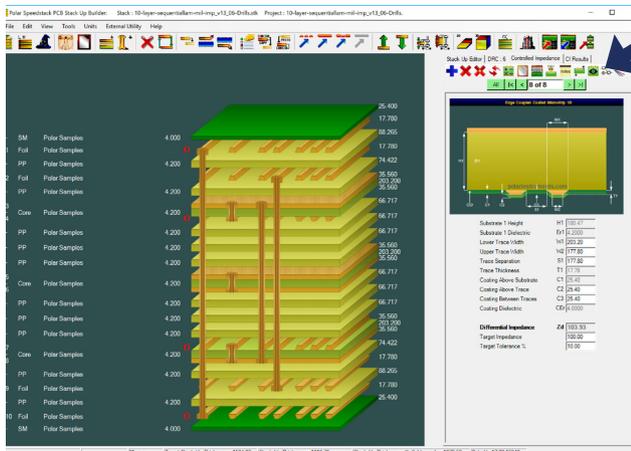
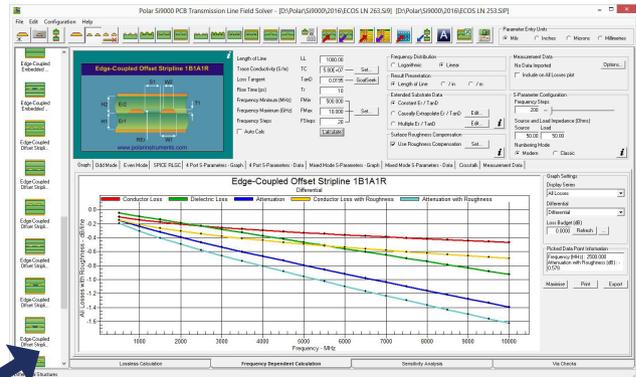
The Si9000e field solving PCB transmission line design system offers advanced field solving methods to model PCB insertion loss and is the natural partner of the Polar Atlas insertion loss test system. Si9000e allows fabricators and designers to explore transmission line design space before committing to build and document the full stackup with Speedstack Si. Insertion loss data is far more extensive than impedance data and Si9000e allows you to import test results from Atlas so you can contrast measured values with modeled predictions.



# Speedstack Si ↔ Si9000e

## Share insertion loss data between tools

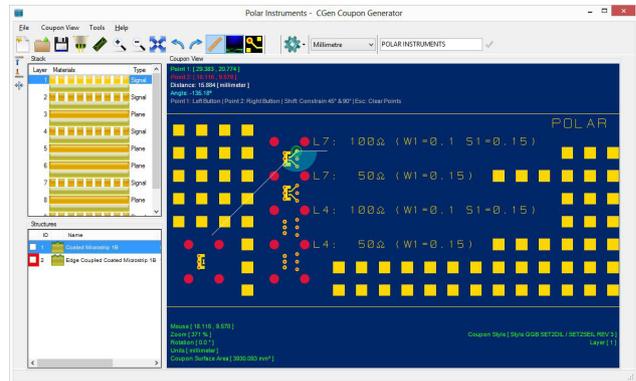
Copy and paste full insertion loss data between Si9000e and Speedstack and vice versa. Either on a structure by structure basis – or take an entire stackup's transmission line data as a project into Si9000e for full analysis with zero data re-entry.



# CGen Si

## Insertion loss coupon generator

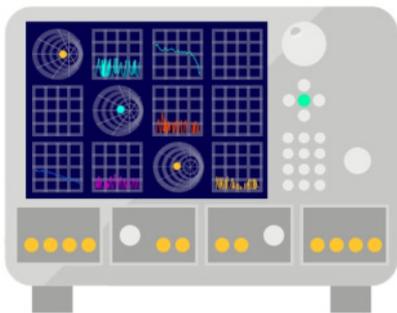
CGen Si creates gerber for popular insertion loss coupons including coupons for both SET2DIL, SPP and Delta-L 4.0 with other styles under consideration. Insertion loss coupons are more complex than impedance coupons, and it is essential for fabricators and PCB technologists to communicate closely when designing loss coupons with CGen Si.



# Atlas Si

## Touchstone file Delta-L 4.0 processor

Atlas Si touchstone file Delta-L 4.0 processor permits OEMs and fabricators to post process long and short line insertion loss touchstone files with the Delta-L 4.0 method to de embed the effects of interconnect from the measurement data. Processed loss information can be pasted back into Si9000e for analysis against solver based models.



Export .s4p files



Import .s4p files



Atlas for Touchstone® processes short and long line .s4p files to compute PCB insertion loss with Delta-L 4.0 Math



### **Polarcare software maintenance and technical support**

With interconnected tools that link not only with each other but also to 3rd party industry standard CAD and CAM systems, Polarcare gives you the peace of mind that your software is updated and secured as technology advances; our experienced staff are proficient at analysing a whole host of PCB transmission line measurement and simulation questions.

### **Licensing**

Polar tools may be licensed to suit your requirements, the clients run on Windows 10 or 11, and the server side on Windows or Linux with the licensing platform being the industry standard FLEXIm. (FlexNet Publisher). Node locked, portable, enterprise, country, continental and global wan licenses are available to suit your specific requirements. Annual licenses are the preferred choice for most customers, and this license type comes with Polarcare included.

### **About Polar Instruments**

Polar Instruments is a market leader in designing and manufacturing tools to simplify and enhance the design, fabrication and testing of printed circuit boards (PCBs). Their innovative tools include the industry-standard Controlled Impedance Test System (CITS) which provides the global PCB industry with an easy-to-use test system for high-speed digital and RF boards, as well as class-leading tools for fast and accurate design and testing of controlled impedance in PCBs. Polar also leads the industry in tools for automated PCB layer stackup design and documentation. Polar Instruments was established in 1976 and has operations and channel partners in the US, UK, Europe and Asia Pacific. The Polar logo and pixelated strip are copyright Polar Instruments Ltd.

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