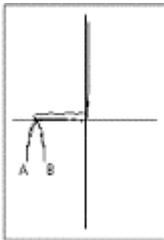


When using ASA to test digital devices you will sometimes encounter difficulty achieving stable signatures. Knowing how the ASA fault locator tests devices can help you develop techniques to reduce spurious FAIL results for good devices.

ASA signature stability

When using Analog Signature Analysis to locate faults in a circuit you may find it difficult under certain conditions to achieve stable signatures. You may even find for example that a device alternates between a PASS and a FAIL on repeated tests.

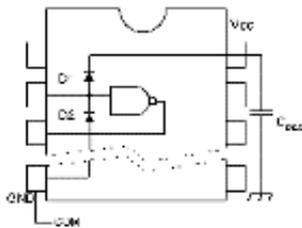


Unstable digital IC signature

Observing the signatures using Live Instrument you may notice "jitter" on the screen as signatures jump between two or more shapes. This phenomenon will probably occur most often when testing digital ICs. It will produce effects similar to the signature in the diagram below where the portion of the signature in the lower left quadrant switches rapidly between the shapes A and B.

Instability or oscillation in signatures are often the result of capacitive circuits and can be reduced by using the fault locator's facility to insert a delay prior to each test - (the Pre Charge function on the PFL series fault locators, the Step Rate function on the T-series fault locators).

Sometimes, however, a rapidly changing signature is the result of the combination of circuit configuration and the method the fault locator uses to produce the signature.



Typical IC input protection and decoupling

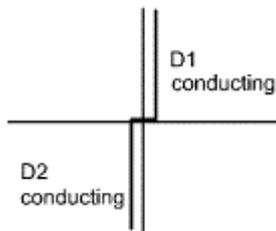
Noise reduction decoupling

Consider a typical digital IC under test as it appears to the fault locator.

Note the decoupling capacitor on the Vcc pin of the IC. Many digital circuits utilise an even distribution of decoupling capacitors to assist in reducing noise, much of which is locally generated (e.g. by local lead inductance). Commercial circuits will typically employ one decoupling capacitor for each digital device.

Testing the device using ASA

During IC testing the fault locator sequentially scans the pins of the IC and applies a sine wave stimulus between each pin under test and COM. Each pin will be stimulated by several sine wave cycles, the actual number will depend on the test frequency, the number of test ranges employed for the test and any delay specified.



In the diagram to the left, as the NAND input pin is tested the sine wave drive voltage causes D1 and D2 to conduct on alternate half cycles to produce the characteristic digital IC signature

However, as D1 conducts during the positive half-cycle of the drive voltage it will allow charging current to flow in CDEC, the decoupling capacitor for the device. (Other decoupling capacitors on the supply line will appear in parallel with CDEC.)

Idealised signature for input protected IC

The voltage on Vcc will therefore rise as CDEC is charged. Under some combinations of test voltage range and circuit configurations Vcc may rise enough to turn on portions of the IC - the current drawn will immediately discharge CDEC. This sequence of events represents a rapidly changing impedance at the node under test and causes the impedance signature to appear unstable. You'll probably find the effect most pronounced when a high current capacity range such as the LOW voltage range is included in the test.

Producing stable signatures

You can significantly reduce or even eliminate this problem by connecting both Vcc and GND to a COM connection - CDEC is effectively short circuited and the two protection diodes appear in parallel.

CAUTION: If you are using an ASA/ICT fault locator such as the PFL series or TD8000 it is common practice to combine ASA and ICT into a single test. Because of the way the fault locator switches between ASA and ICT it is essential that you use both COM lines, i.e. connect the board GND to the left COM socket and Vcc to the right COM socket.



Polar Instruments Ltd
Garenne Park, St Sampson, Guernsey, Channel Islands GY2 4AF, UK

www.polarinstruments.com
mail@polarinstruments.com
Tel: +44 1481 253 081 Fax +44 1481 252 476

© Polar Instruments 2001. Polar Instruments pursues a policy of continuous improvement. The specifications in this document may therefore be changed without notice. All trademarks recognised.